ELEC 3106
Study Notes

By Tommy Sailing

Semester 1 2013 – Electrical Engineering
The University of New South Wales

NOTICE:
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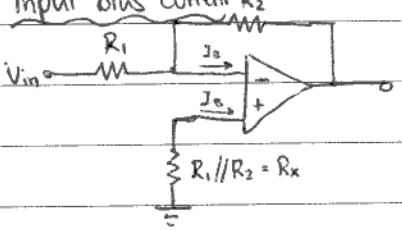
NOTES: Tidbits of electronical knowledge (or a glossary, of sorts)

Input bias current



- R_x exists to guard against a systematic offset from the bias current.
- $V_o = I_B \left(R_2 - R_x \left(1 + \frac{R_2}{R_1} \right) \right)$

($\frac{R_2}{R_1}$: inverting gain)

- Because we want $V_o = 0$, we can rearrange this so that $R_x = \frac{R_2}{1 + R_2/R_1} = R_1 // R_2$.

Powersupply rejection ratio and commonmode rejection ratio

Because op amps are often used in mixed signal circuits (analogue and digital), ripple from digital switching might end up corrupting the power supply. These error voltages might wind up corrupting the output of the amplifier.

PSRR is RATIO OF DIFFERENTIAL GAIN to GAIN EXPERIENCED BY CHANGE IN POWER SUPPLY.

$$PSRR^+ = \frac{A_d}{A_+}$$

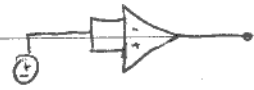
$$PSRR^- = \frac{A_d}{A_-}$$

$$A_d = \frac{V_o}{V_i}$$

$$A_+ = \frac{V_o}{V_{dd}}$$

$$A_- = \frac{V_o}{V_{ripple}}$$

An ideal op amp will output nothing when both inputs are at the same common mode potential:



$V_{out} = 0$! However, real circuits do no such thing.

$$CMRR = \frac{\Delta V_{cm}}{(\Delta V_{out} / A_v)}$$

Error in CM voltage referred to nominal output.

Input/output voltage range

- Input voltage range is constrained as range of voltages over which CMRR is met.
- Output voltage range is likely to be close to the rails (rail-to-rail output) allow perhaps a 100-150 mV buffer when quoting this range.

NOTES: Tidbits (cont...)

Total Harmonic Distortion

- Just remember this formula: $THD = \frac{\sqrt{V_2^2 + V_3^2 + \dots}}{V_1}$
- V_1 is the tallest (fundamental freq)

Maximum fan-out

- Maximum fan-out is defined by the absolute values of: $\min\left[\left(\frac{I_{OL}}{I_{IL}}\right), \left(\frac{I_{OH}}{I_{IH}}\right)\right]$

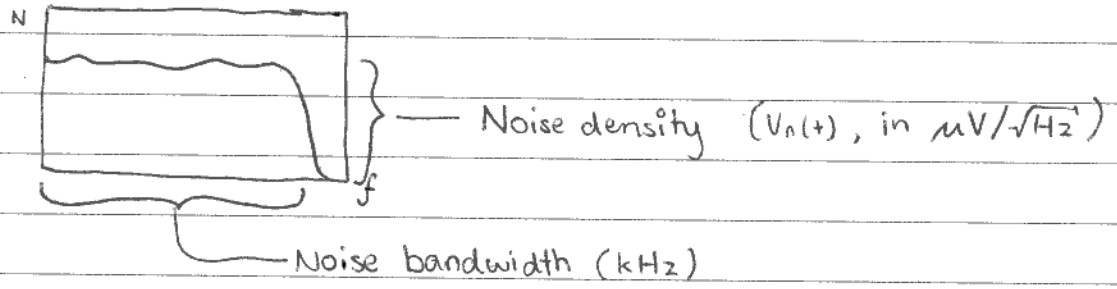
Noise margins (voltage)

- $NMH = V_{OH} - V_{IH}$ (Low! input! first!)
- $NML = V_{IL} - V_{OL}$

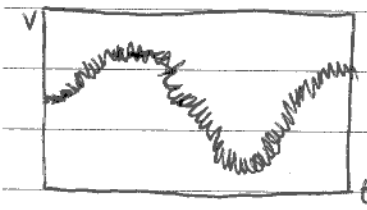
Transition times & speed

Consider maximum length of a wire interfacing a digital logic family. Ensure that transmission line effects (a pain in the back-side) do not need to be considered - make sure that $T_t \times C$ (transition time × speed) is much larger than maximum length.

Noise spectral density



RMS output noise, $V_{No\,RMS} = \sqrt{V_n^2(+) \cdot B_N}$



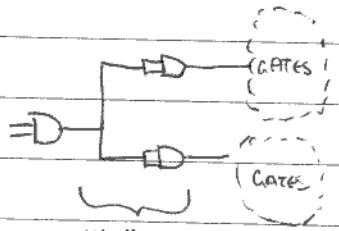
Y-T trace · get width of noisy trace

$V_{rms(noise)} = \frac{width}{6}$ as std. dev ~ 6σ.

NOTES: Tidbits

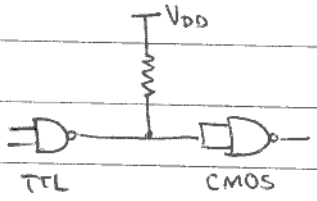
Preventative circuit design

- TTL circuit about to reach fan-out limit



split the fan-out

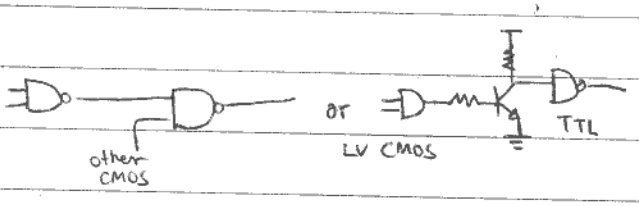
- TTL/CMOS interfacing



A pull-up resistor is required. (often ~10kΩ or so)

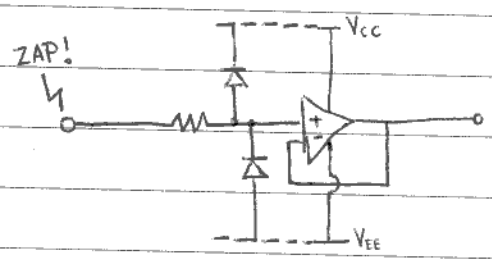
~~No more~~

- CMOS/TTL interfacing



Low voltage CMOS to TTL requires a common-emitter amplifier to bring the voltage to acceptable levels.

- Adding ESD protection to an op-amp circuit



ESDs are normally 1000s of volts, connecting a diode between the rails means if the input voltage exceeds supply rail voltages the (massive) input will short circuit to one of the supply rails, leaving the delicate electronics untouched.

NOTES: Tidbits

Slew rate

$SR = 2\pi f V_{max}$ (V/s) Always remember to stay within SI units.

Logic gate manufacturing

Digital logical gates may have three different sorts of outputs:

i. Open-drain: Has two possible output states, pull-down (low) and open circuit.

ii. Tri-state: Has three output states, pull-down, pull-up and open circuit.

iii. Normal: Has two output states, pull-down and pull-up.

CMOS vs TTL

- CMOS is more expensive at chip level, but as a whole CMOS chips get cheaper as part of a large system due to their smaller manufacturing process.
- TTL circuits draw (and dissipate) more power at rest, ~~but~~ low clock speeds. At high clock speeds CMOS power consumption increases.
- CMOS chips are ideal for digital signal transmission due to longer rise and fall times.
- CMOS chips are more sensitive to ESD damage than TTL chips.

LM7805 hold up-time

~5V regulator $C_{res} = 5000\mu F$ $I \simeq 1A$ dc

$V_{in,dc\,(min)} \simeq 10V$

Min input to regulator = 7.45V

$\therefore t_{hold-up} = \frac{(10 - 7.45) \times 5 \times 10^{3} \times 10^{-6}}{1}$

$\simeq 13$ ms