ELEC 3106
Study Notes

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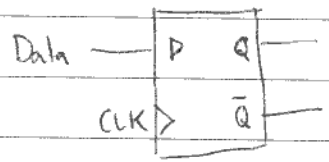
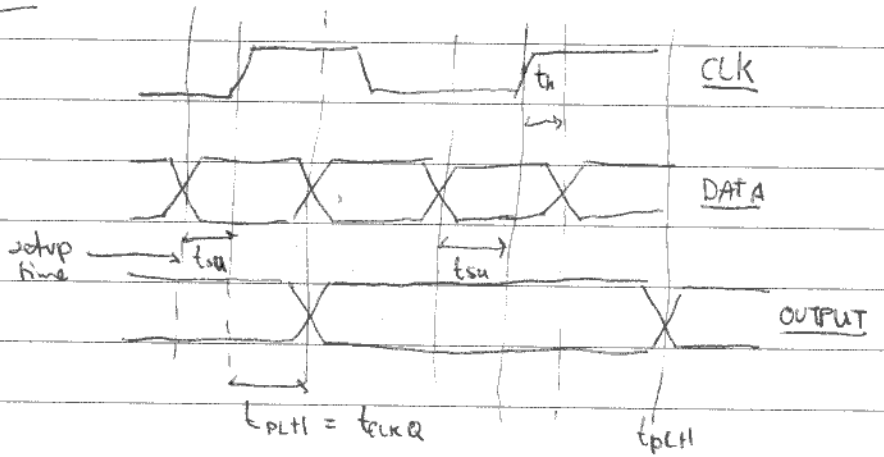
Semester 1 2013 – Electrical Engineering
The University of New South Wales

Setup time & hold time in Flip Flops

- Consider a D Flip flop.



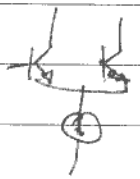
Rising edge clocked



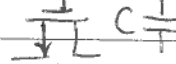
Setup time t_{su} : just before clock edge

hold time t_h : just after clock edge.

Emitter coupled logic draws substantially more current. Bipolar.

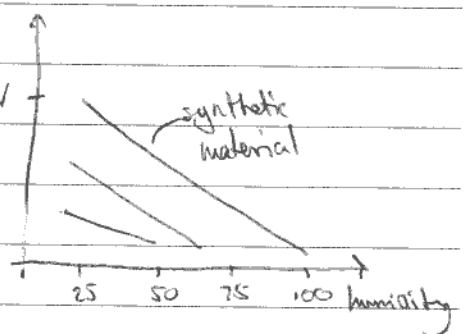


ESD

(CMOS)  $C = Q/V$ How many e^- do you need for V to be -15V? eh? across the gate.

conditions for ESD:

* low humidity
* rubbing surface on synthetic material.



NOTES: Week 4 - Logic Interfacing

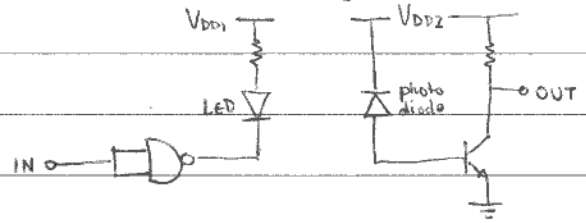
Isolation

- Galvanic isolation means no metal conductor connecting 2 circuit boards.
- It is safest to keep power rails within the bounds of the equipment case.

→ Enter the OPTO-COUPLER

↳ LED chip integrated with photodiode / phototransistor, optically coupled.

↳ One is needed per digital channel.

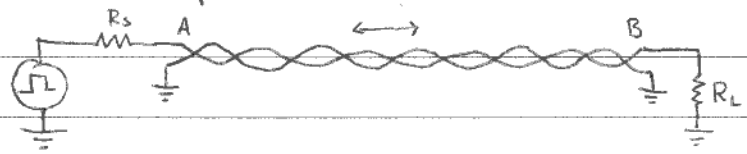


The idea is to keep V_{DD2} isolated from V_{DD1}.

↳ Opto-couplers unfortunately are low-speed (100kbit/s, switching times 2-5μs) unless you pay lots, they use up a lot of power on the isolated side and need several passive components + buffer gate to logically interface.

Digital signals over distances

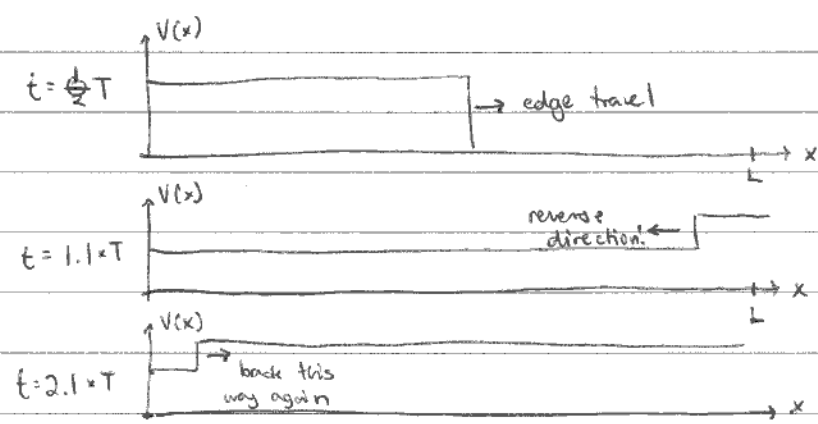
- Consider a twisted pair transmission line:



Where characteristic impedance = $Z_0 \neq R_S \neq R_L$ and time for A → B = T.

↳ Reflection coefficient at load $\Gamma_L = \frac{R_L - Z_0}{R_L + Z_0}$

↳ Reflection coefficient at source $\Gamma_S = \frac{R_S - Z_0}{R_S + Z_0}$



NOTES - Week 4: Logic Interfacing

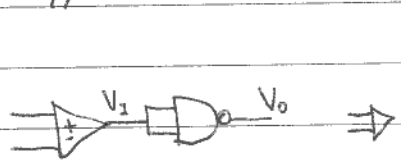
Analogue-Digital Interfacing

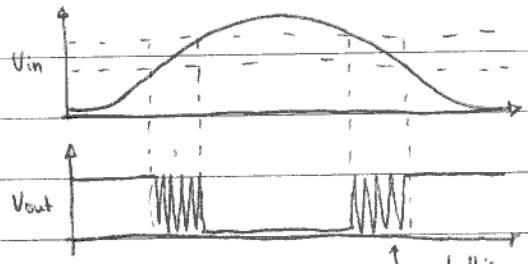
PROBLEMS: preventing digital switching noise from contaminating analogue signal
interfacing wide range of analogue input voltages to digital circuit

Rule #1: SEGREGATE ANALOGUE & DIGITAL CIRCUIT BLOCKS!

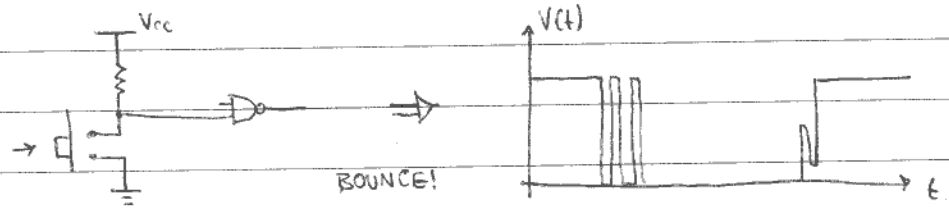
↳ Generating digital levels from analogue signals
- ↳ Always use comparator or Schmitt trigger
- ↳ NEVER feed analogue signals into TTL or CMOS gates.

Why? Analogue signals are SLOW, logic gates need slew rates faster than 5V/μs otherwise oscillation occurs:



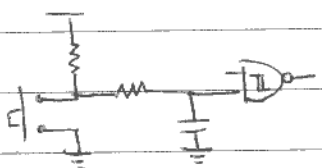


↳ Generating digital signals from humans
- ↳ Even slower than analogue signals! Often mis-triggers clock circuits.

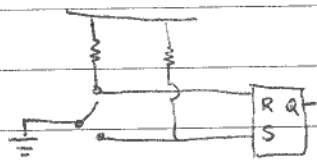


↳ Solution: debounce circuits

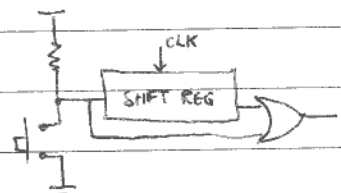
- RC: deliberately slows rise time. Input must be ST.



- SR FF:



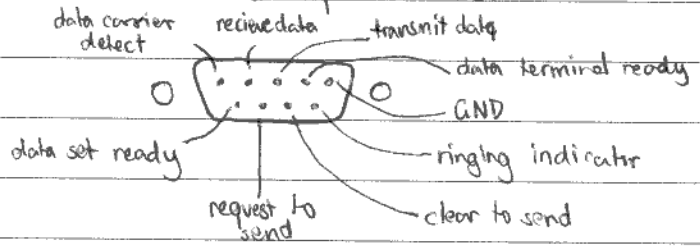
- SHIFT REGISTER



IC, LOGIC & CMOS GATE DESIGN

Data Interchange Standards

RS-232 & RS-422 are ubiquitous. Superseded by EIA-232 & EIA-422, they are standard logic interfaces not suited to driving long lines. There is often too much reflection and has low noise immunity. So, we use these 'classic' set of standards. You can see this ugly bastard on a 90's PC:



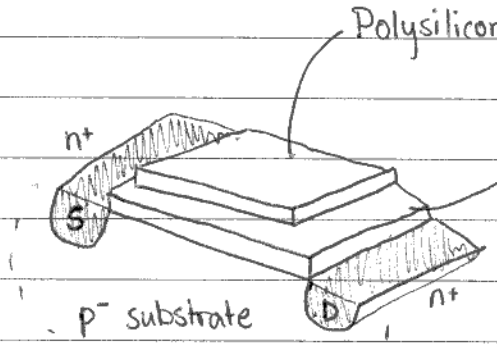
JUST USE EIA-485, CAN, USB or Ethernet!

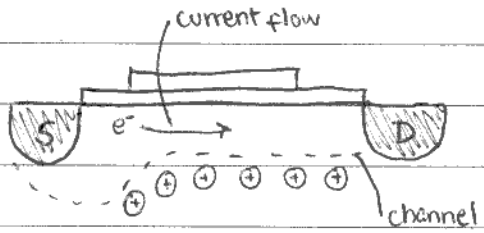
and... its electrical characteristics!

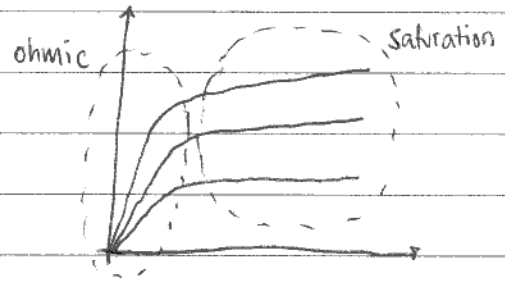
	RS/EIA-232	422
Line type	unbalanced	balanced (differential)
Line impedance	N/A	~ 100Ω
Max line length	load dependent, ~15m	$L \simeq 10^5/B$ meter (B=baud)
Max Data rate	~20kB/s	10 MB/s

NOTES : Week 4 - CMOS design

CMOS gate design

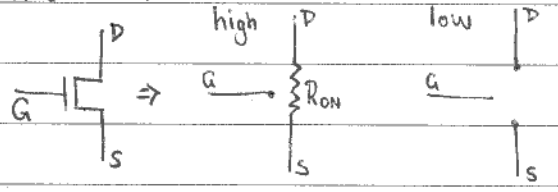


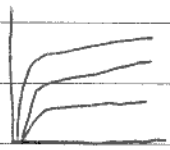




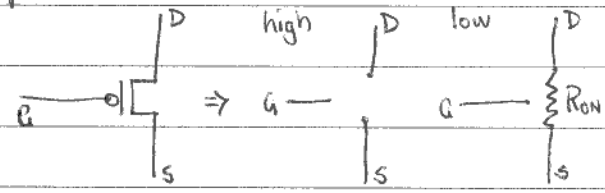
MOSFETS as circuit elements

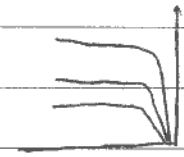
n-channel





p-channel

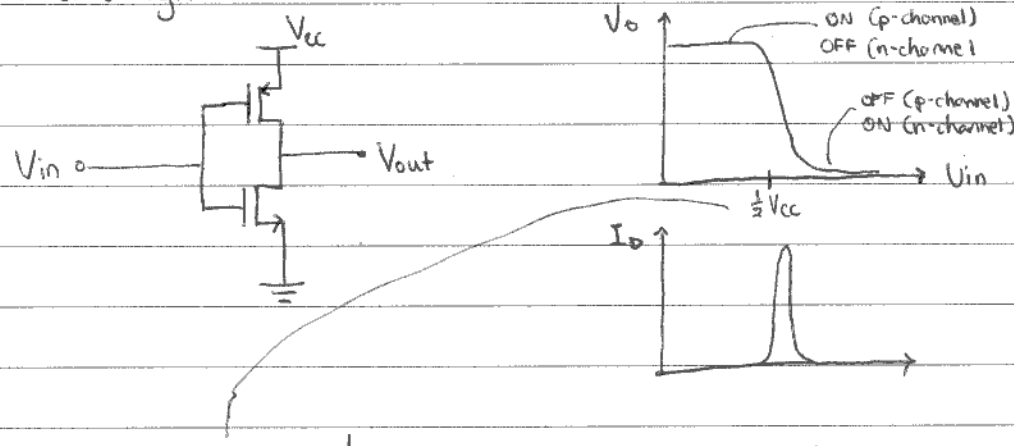




- in both cases, $R_{ON} = \frac{1}{\beta (V_{cc} - V_{th})}$ ← threshold voltage, not to be confused with thermal voltage!

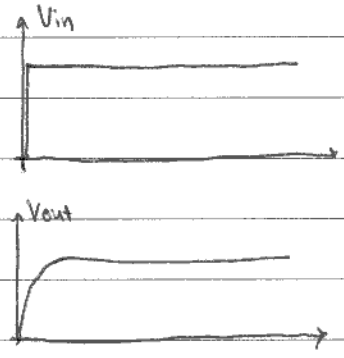
NOTES: Week 4 - CMOS design

↳ inverter design



note that if $V_{in} = \frac{1}{2} V_{cc}$, both n- and p-channel type MOSFETs are on at the same time, resulting in a spike in current as shown below.

↳ inverter propagation delay



Assumption: time the transistor spends in saturation mode is negligible.

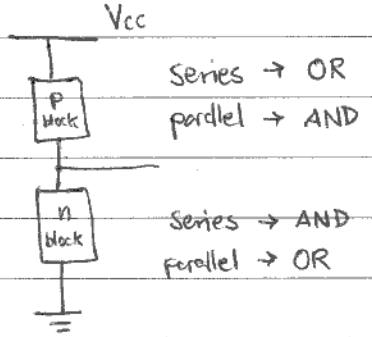
time constant $\tau = R_{ON} \times C_L$

so $V_{out}(t) = V_{cc}(1 - e^{-t/\tau})$

$\therefore$ after some magic, $t_{PLH} = \ln(2) \times \tau$

$t_{THL} = \ln(9) \times \tau$

↳ building logic gates from MOSFETS



Series → OR
parallel → AND

Series → AND
Parallel → OR

For more detail, revise ELEC 2141 notes!