ELEC 3106
Study Notes

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The University of New South Wales

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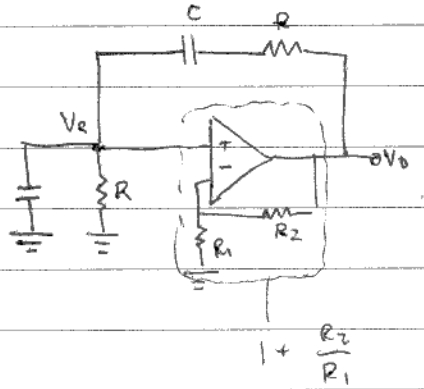
Week 11 - Oscilliators

RC Wein Bridge

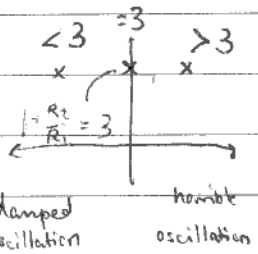


- Phase shift oscillator.
- Loop gain $V_+ \to V_a$

$$T = \left(1 + \frac{R_2}{R_1}\right) \frac{R \,/\!/\, \frac{1}{sC}}{R + \frac{1}{sC} + R \,/\!/\, \frac{1}{sC}}$$

$$= \frac{1 + \frac{R_2}{R_1}}{3 + j\left(\omega RC - \frac{1}{\omega RC}\right)}$$ imaginary part → 0.

- Loop gain $T = 1$ when $\omega = \omega_0 = \frac{1}{RC}$ and $1 + \frac{R_2}{R_1} = 3$
- Poles exist on the imaginary axis of the s-plane.

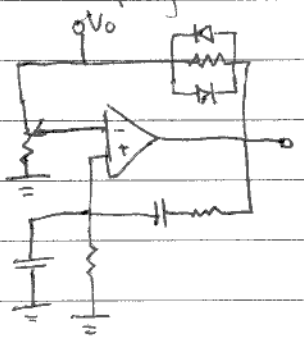


Consider:

- Is the output of the op-amp saturated (over time), so the amplitude must be controlled
- Drops in gain as output of op-amp saturates, causing distortion on your waveform. - poor single-frequency spectrum = harmonics galore.

- How do we limit amplitude with out saturation on opamp output?

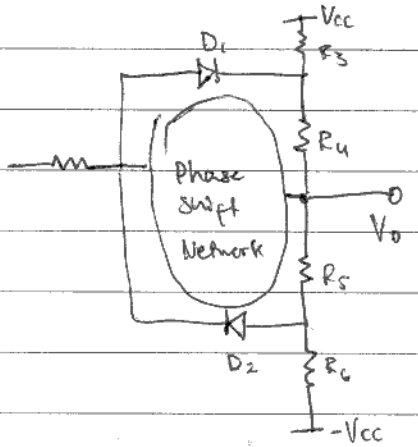
↳ Diodes clamping a resistor:



When $V_o \gg 0$ or $V_o \ll 0$ D_1 or D_2 will conduct, shorting out R_f, controlling the gain of the amplifier.

↳ Apply non-inverting amplifier topology and connect string of resistors + diode clamp to the output.

NOTES: Week 11 - Oscillators



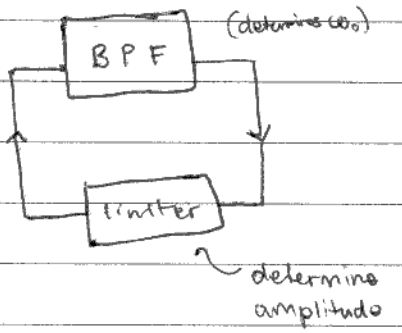
To sustain oscillation:

- $V_o >> 0$ - positive peak
- When $V_o > V_1$, D_2 will conduct
- $V_D = -V_{cc} + \frac{R_f}{R_5 + R_6}(V_o + V_{sc})$

$\left(V_1 \simeq \frac{1}{3}V_o\right)$ $(R_2 \simeq 2R_1)$

- $V_o << 0$, consider V_a - negative peak.

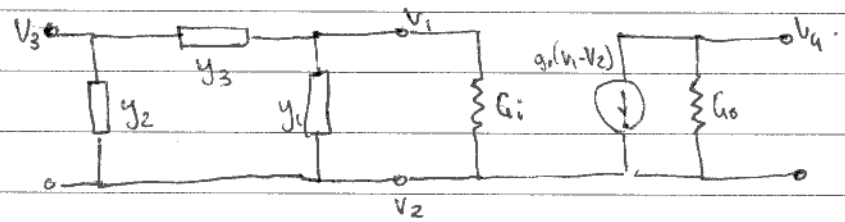
Sinusoidal oscillator design



- Dependent on a sharp bandpass filter
- Oscillator frequency limited by:
  - ↳ op-amp gain bandwidth. ($\simeq$ 10 MHz)
  - ↳ high frequency - R & C values are small, small capacitors may be parasitic on PCBs.
  - ↳ if using transistors → limited by f_T (>> op amp gain bandwidth)

We get high frequency oscillator networks with LC networks and transistors. RC type are not suitable for GHz range of frequencies.

Generic Oscillator



KCL at nodes

$$\begin{bmatrix} y_1+y_2+G_i & -y_1+G_i & -y_3 & 0 \\ -(y_1+G_i+g_m) & (y_1+y_2+G_i+G_o+g_m) & -y_2 & -G_o \\ -y_3 & -y_2 & y_2+y_3 & 0 \\ g_m & -(G_o+g_m) & 0 & G_o \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

NOTES : Week 11 - Oscillators

Consider a common-emitter BJT and $V_3 = V_4$, and $G_o = 0$

↳ this actually gives a feedback path

↳ $$\begin{bmatrix} y_1 + y_2 + G_i & -y_3 \\ g_m - y_3 & y_2 + y_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

↳ If the circuit oscillates, we say $V_1, V_3 \neq 0$!
And the determinant must be equal to 0.

- Let $y_1 = j\frac{1}{X_1}$ $y_2 = j\frac{1}{X_2}$ $y_3 = j\frac{1}{X_3}$ (reactive elements)
→ we don't know which one is which!

→ substitute in $\Delta = (Y_1 + Y_2 + G_i)(Y_2 + Y_3) - (g_m - Y_3)(-Y_3) = 0$
and find the real part $Re\{\Delta\} = 0$ and $Im\{\Delta\} = 0$

→ this means $X_1 + X_2 + X_3$ also adds up to 0. We also extract

$$X_1 = \left(\frac{g_m}{G_i}\right) X_2 \qquad \left(\frac{g_m}{G_i} \text{ is real and positive}\right)$$

↳ from X_1 & X_2's relationship, X_2 is the same sign as X_1.
it also means X_1 & X_2 are the same type of reactive element.
↳ as $X_3 = -(X_1 + X_2)$, X_3 must be the other kind of reactive element.

Now let $X_1 = -\frac{1}{\omega_0 C_1}$; $X_2 = -\frac{1}{\omega_0 C_2}$; $X_3 = \omega_0 L_3$.

Solving, $$\omega_0 = \sqrt{\frac{1}{L_3}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)}$$ (Collpitts Oscillator)

And for oscillation,

$$X_1 \leq \frac{g_m}{G_i} X_2 \quad \rightarrow \quad \frac{C_2}{C_1} \leq \frac{g_m}{G_i}$$

NOTES: Week 11 - Oscillators

If we make X_1 & X_2 inductive, and X_3 capacitive;

$$X_1 = \omega_0 L_1 \; ; \quad X_2 = \omega_0 L_2 \quad \text{and} \quad X_3 = -\frac{1}{\omega_0 C_3}.$$

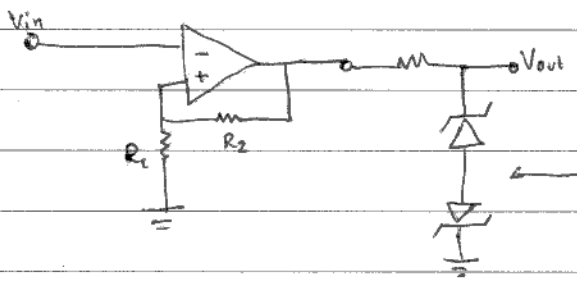
$$\omega_0 = \sqrt{\frac{1}{C_3}\left(\frac{1}{L_1}+\frac{1}{L_2}\right)} \quad \text{and} \quad \frac{L_1}{L_2} \geq \frac{g_m}{G_i} \qquad \text{(Hartley oscillator)}$$

- The original and traditional LC oscillators!

Non-ideal case

- Suppose inductor L has a resistance R $\rightarrow$ $y_3 = \dfrac{1}{R+j\omega L_3}$
- Consider a Collpitts oscillator. Show $\omega_0 = \sqrt{\dfrac{1}{L_3}\left(\dfrac{1}{C_1}+\dfrac{1}{C_2}+\dfrac{G_i R}{C_1}\right)}$
- Condition for oscillation: $\dfrac{R}{G_i} \leq \dfrac{1+g_m/G_i}{\omega_0^2 C_1 C_2} - \dfrac{L_3}{C_1}$

Schmitt Trigger



$$V_{out} = \begin{cases} V_{OH} \\ V_{OL} = -V_{OH} \end{cases}$$

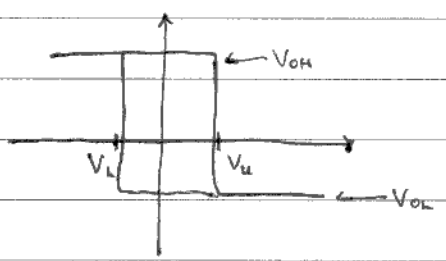
clamp output to avoid op-amp set by Zener voltages.

+ve saturation voltage $\neq$ -ve saturation voltage

so, clamped, $V_{OH} = \underbrace{V_Z}_{\text{Zener breakdown}} + \underbrace{V_F}_{\text{forward voltage of diode}} = -V_{OL}$

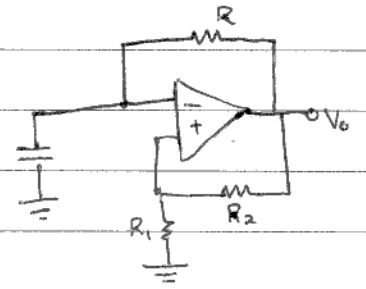
$$V_{OUT} = V_{OH} \rightarrow V_+ = \frac{R_1}{R_1+R_2} \times V_{OH} = V_U$$

$$V_{OUT} = V_{OL} \rightarrow V_+ = \frac{R_1}{R_2+R_1} \times V_{OL} = V_L$$

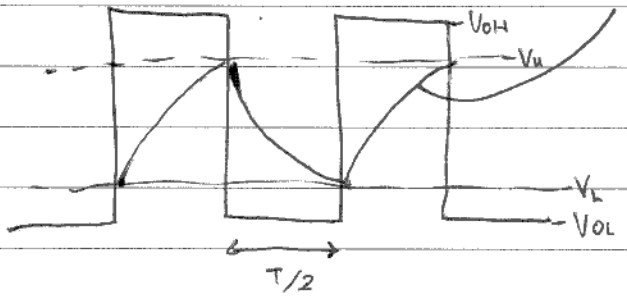


NOTES: Week 11 - Oscillators

→ S.T. Oscillator



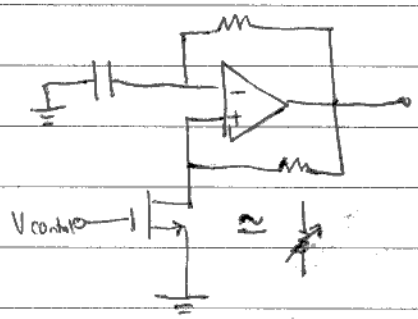
- R_1 & R_2 influence switching limits (frequency)
- $V_{OH} = -V_{OL}$ and $V_u = -V_L$

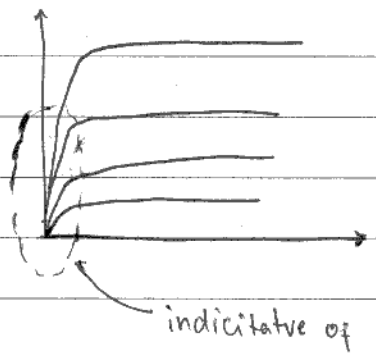


Capacitor charging & discharging

$$T = 2RC \ln\left(\frac{2R_1 + R_2}{R_2}\right)$$

→ Voltage controlled oscillator





indicitative of transistor output resistance.

$$I_D = K\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

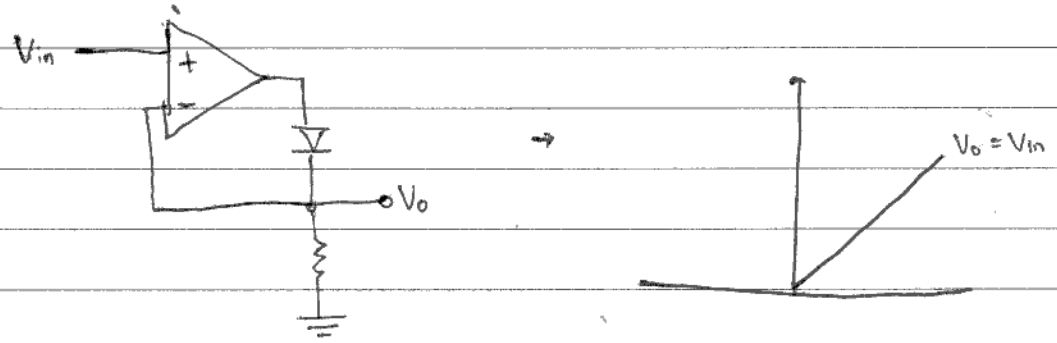
$$\frac{1}{r_{ds}} = \frac{\partial I_D}{\partial V_{DS}} = K(V_{gs} - V_{th})$$

$$\rightarrow T = 2RC\ln\left(1 + \frac{2}{\beta R_2 (V_{as} - V_{th})}\right)$$

Very large changes in V_{as} until large changes in the period due to it being a log function.

NOTES: Week 11 - Oscillators

Precision Rectifier

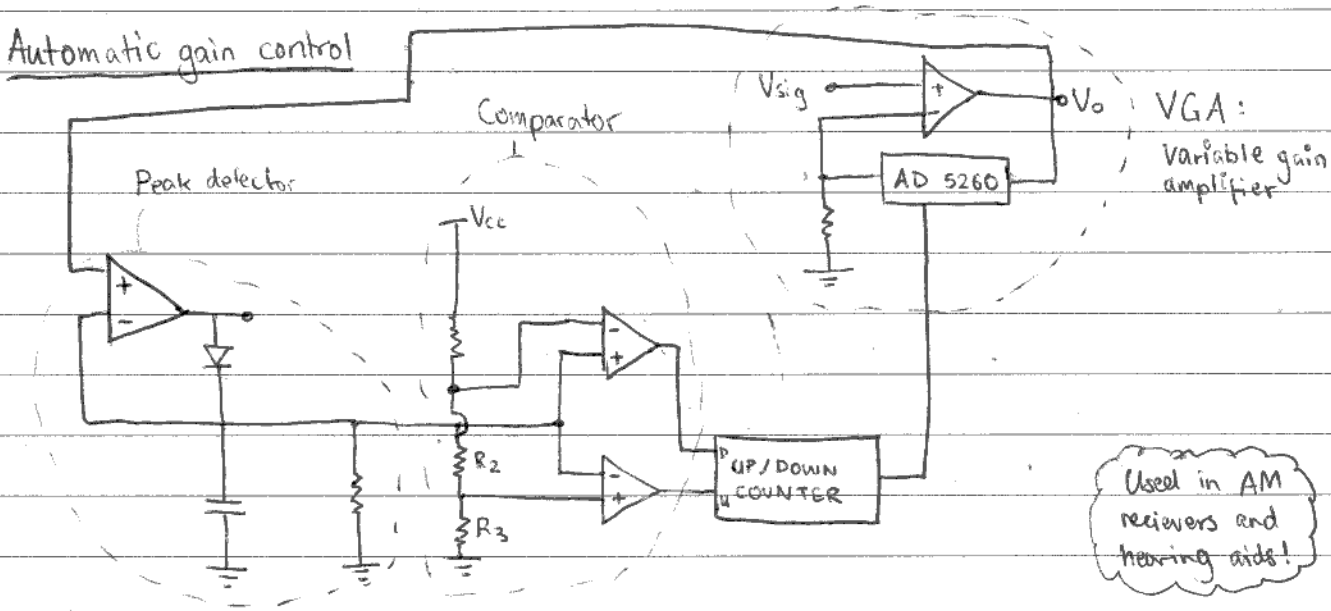


Result: Half-wave rectifier.

$V_+ > V_-$ ... $V_{in} > 0$? $V_o = V_{in}$

$V_+ < V_-$ $V_{in} < 0$? $V_o = 0$ (because the diode is off)

Automatic gain control



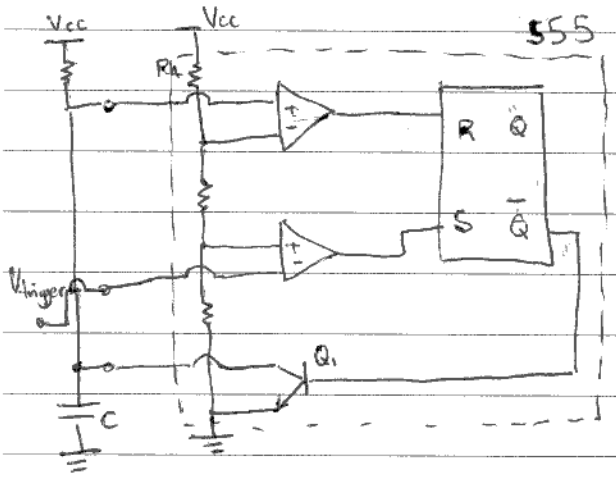
Essential elements:

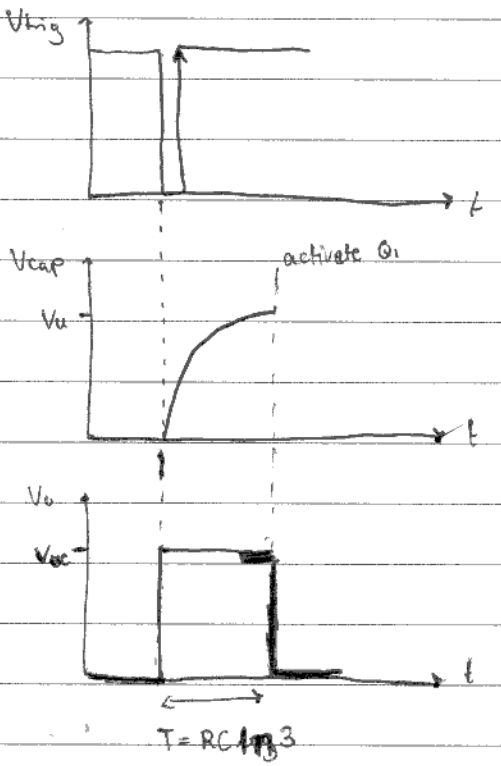
- VGA → combination of op-amp and AD5260 chip (R_2 resistor)
- Peak detector (on left) → must discriminate levels of peaks you have detected
- Comparator and up-down counter performs the above.

Input signal passes through VGA to produce an output level, fed to the peak detector, to be stabilised by the AGC circuit. The peak detector detects output level and compares with the set point (determined by resistor chain R_1, R_2, R_3). Error signals are generated from the comparison, and drive the up-down counter - which increases/decreases the AD5260 "resistance". Increase gain for weak signals and vice versa.

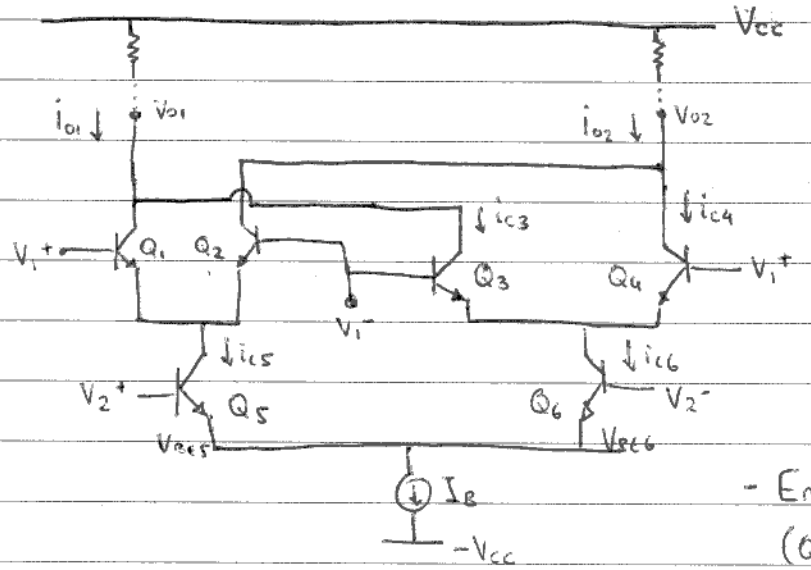
NOTES: Week 11 - Oscillators

Monostable (one-shot)





Gilbert Multiplier



- A popular analogue multiplier. The output current is an accurate product of the differential base currents of both inputs.

- Consists of two differential amplifier stages:
  - Emitter-coupled transistor pairs (Q_1/Q_2, Q_3/Q_4) whose outputs are connected (summing their currents). The emitter junctions are fed by the collectors of Q_5 and Q_6, whose output currents become emitter currents for the differential amplifiers.

$$i_{C6} = \frac{I_B}{1 + e^{V_{2d}/V_T}} \qquad i_{C5} = \frac{I_B}{1 + e^{-V_{2d}/V_T}} \qquad \left(V_T = \frac{kT}{W}\right)$$

NOTES: Week 11 - Oscillators

Phase detector

Assume two signals with the same frequency but differ in phase:

$V_1 = A \sin(\omega_1 t)$

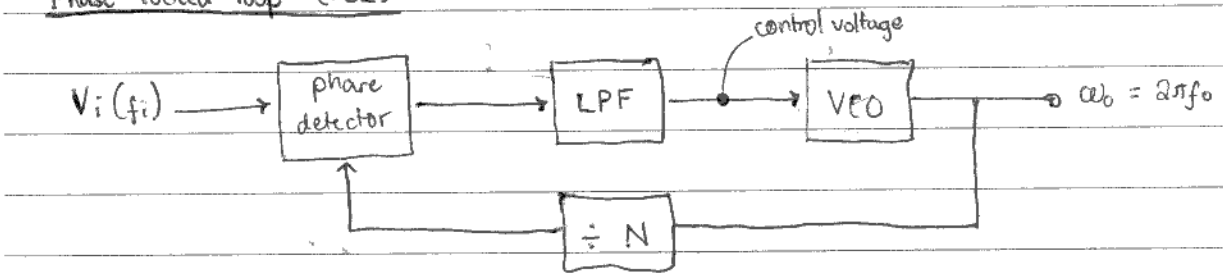
$V_2 = B \sin(\omega_1 t + \phi)$

multiplier output: $V_o = \frac{kAB}{2}\cos(\phi) - \frac{kAB}{2}\cos(2\omega_1 t + \phi)$

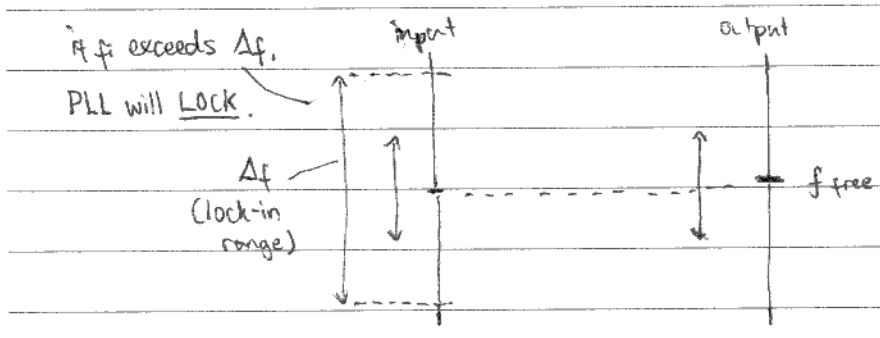
dc output ∝ phase difference through cos() — remove, with LPF.

- phase difference is the output voltage! If we want $\theta_E = 0$, make $\phi = \frac{\pi}{2} = 90^\circ$.
- if small, $\theta_E \simeq \frac{kAB}{2} \cdot \Delta\phi$, but may be valid for larger $\Delta\phi$.

Phase locked loop (PLL)



A PLL is a form of oscillator whose frequency is locked onto some frequency of an input signal. It is a negative feedback system. Under a locked condition, $f_o = f_i$, the phase of the 2 signals are matched, and range f_i can vary and f_o will track according before f_i and f_o, this range is called lock-in range - f_o and f_i can no longer be equal.



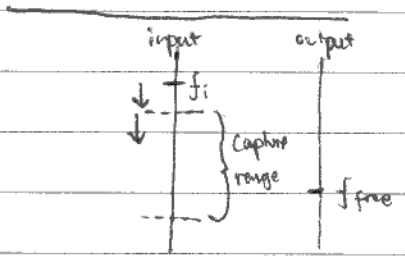
Dependent on components, filter and VCO.

NOTES: Week 11 - Oscillators

When PLL is not in lock:

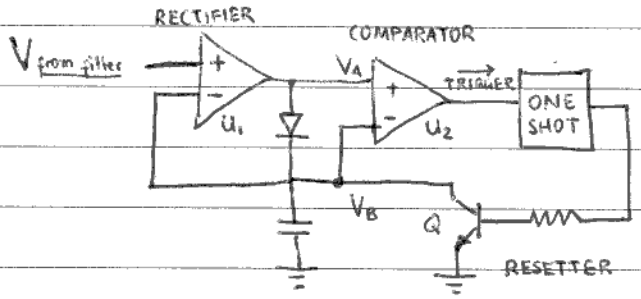
↳ $f_o \neq f_i$

↳ when f_i enters capture range, f_o will watch f_i and then get locked.



Used in communication systems, FM demodulation, clock data recovery and frequency synthesizers.

Peak detector



Operation:

- When $V_{filter} > V_B$, the amp output V_A is pulled-up to make $V_B = V_{FILTER}$.
- When $V_{FILTER} < V_B$, the op-amp output sinks but V_B is unchanged because of C.

So the circuit components U_1, D and C act as an ideal peak detector. The comparator, U_2, detects when D is conducting (when a new peak value is found). When this happens, its output is high, triggering the one-shot. This forces one shot's output to be low, turning Q off.

When $V_A < V_B$ (so $V_{filter} < V_B$), the comparator keeps its output low. If it's been low for more than a time T, the one shot goes high, saturating Q and discharging V_B to ground.

The resultant action is V_B holding the maximum value that V_{FILTER} has taken for the past T seconds.