

ELEC 3106

Study Notes

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Semester 1 2013 – Electrical Engineering
The University of New South Wales

NOTICE:

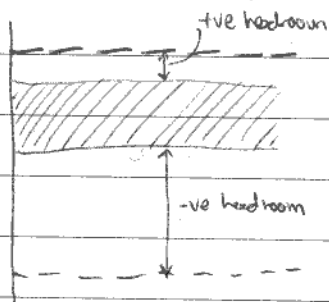
These are my personal study notes, written as an undergraduate university student, based on the course content of ELEC 3106, 2013 and are provided only in the hope that you will find them useful for your own personal studies. They are not to be treated as a formal, peer-reviewed publication and may contain errors. As such, do not rely on these notes as a 100% reliable study source. I politely ask that these notes are not distributed outside of my website, www.tommysailing.com.

Non-idealities of op amps

Offset voltage: V_{os} - the differential dc voltage required between the inverting and non-inverting inputs of an amplifier to drive its output to zero. Range is generally 10's of mV to 1's of μ V. It appears as an additional "error" voltage in series with the inputs.

$$\boxed{\text{Output offset} = \text{Input offset} \times \text{CL gain !!}}$$

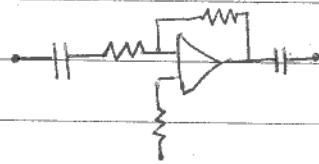
An unwanted effect is **OUTPUT SATURATION DUE TO AMPLIFIED OFFSET.**



- Tiny amount of headroom for one polarity

- Huge amount for the other. = Distortion

Fixing it:

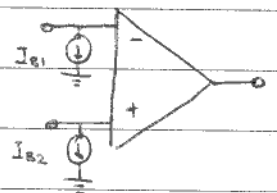


AC coupling (capacitive coupling) gives a DC gain of unity so $V_{os} = V_{ios}$.
But cap charging = power-on delays.

Offset drift: Related to temperature & time. Rule of thumb: $3.3 \mu\text{V}/^\circ\text{C}$.

Bias & Offset Currents: Input bias current is the average DC current required by the inputs of the amp to establish correct bias conditions in the first stage. Input offset current is the difference in bias current requirements of the two input terminals.

$$I_{os} = |I_{B1} - I_{B2}| \quad \left| \quad \text{On average } I_B \approx 100\text{nA}, I_{os} = 10\text{nA} \right.$$



I_B & I_{os} determine the steady state input impedance of the amp & result in additional voltage offsets. But irrelevant for CL inverting, since feedback makes input impedance ≈ 0 .

NOTES - Week 1 : Non-idealities of op amps

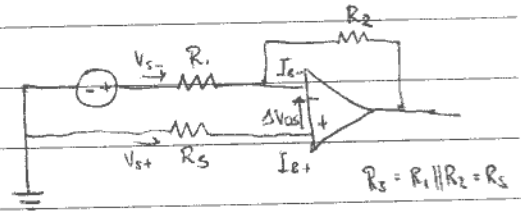
Output offsets as a result :

• Ideal : I_B & R_S equal

$$V_{st} = V_s = I_B \times R_S \quad | \quad \Delta V_{os} = 0$$

• Practical : I_B & I_{st} differ by I_{os} , R_S equal

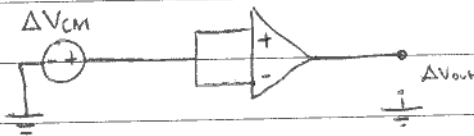
$$V_{st} = I_{st} \times R_S \quad | \quad V_s = (I_B + I_{os}) \times R_S \quad | \quad \Delta V_{os} = I_{os} \times R_S$$



⚠ Keep input resistances equal! This will prevent I_{os} from contributing to offset.

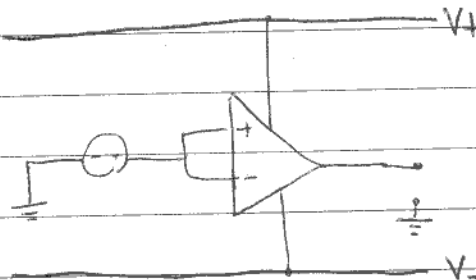
Common-Mode Rejection Ratio (CMRR): Gain differences between inputs and CM offset variations combine to produce an error at the output as the common mode voltage varies. This error is DIVIDED BY THE GAIN to produce a "Common mode error voltage".

The ratio of this voltage to the common mode input voltage is the CMRR. E.g. CMRR of 80dB = input v. error of 100μV for every 1V change at bipolar inputs. Not constant, and worsens with increasing f.



$$CMRR = \frac{\Delta V_{cm}}{(\Delta V_{out} / A_v)} \leftarrow \text{CMEV}$$

Power Supply Rejection Ratio (PSRR): Similar to CMRR but relating to error voltages as a result of fluctuations in power rail voltages.



$$PSRR_+ = \frac{\Delta V_+}{CMEV}$$

$$PSRR_- = \frac{\Delta V_-}{CMEV}$$

Large CMRR is good. Both reduce with frequency (bad!)

NOTES - Week 1 : Non-idealities of op amps

Attempt at Tutorial 1

Slew Rate: Slew rate determines (limits) the bandwidth of the full-power response. It exists because a compensation capacitor must be installed for stability in the high-frequency response. The rate of change of the output voltage is determined entirely by i_{out} and C_c . SLEW RATE IS THE MAXIMUM RATE OF CHANGE POSSIBLE AT AN OP-AMP'S OUTPUT.