ELEC 3106
Study Notes

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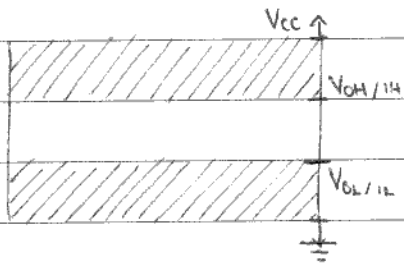
Semester 1 2013 – Electrical Engineering
The University of New South Wales

NOTES - Week 3: Digital fan-out, noise margins, VTC, I/O, gate delays

Basics of digital logic:



Each input is designed so that any voltage below V_{IL} is regarded as logic 0 and any voltage above V_{IH} is regarded as logic 1. Same goes for output.

The space in between is called the 'noise immunity', where the input is undefined. Switching must occur quickly to avoid being in this state (more common in asynchronous circuits!). Allowable range for inputs are generally more generous than those of the inputs.

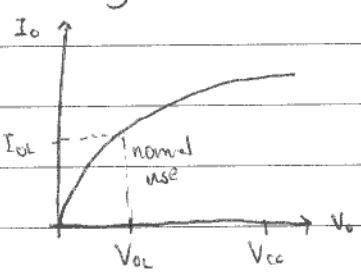
Requirement in DCD: $V_{OH} > V_{IH}$ and $V_{OL} < V_{IL}$

Transistor-Transistor Logic (TTL) levels:	CMOS levels (PS dependent)
74LS00: V_{CC}: 4.5V → 5.5V	74HC00: V_{CC} = 2V → 6V
V_{IH}: 2V V_{IL} = 0.8V	V_{IH}: 1.5V→4.2V V_{IL} = 0.5V → 1.5V
V_{OH}: 2.4V V_{OL} = 0.4V	V_{OH}: 1.9V→5.9V V_{OL} = 0.1V→0.4V

We prefer CMOS circuits that are TTL-compatible, e.g. 74HC family. TTL devices consume substantially more power than CMOS devices. When input is pulled low, lots of current flows out. When high, little current flows in.

And noise margins: $NMH = V_{OH} - V_{IH}$ & $NML = V_{IL} - V_{OL}$

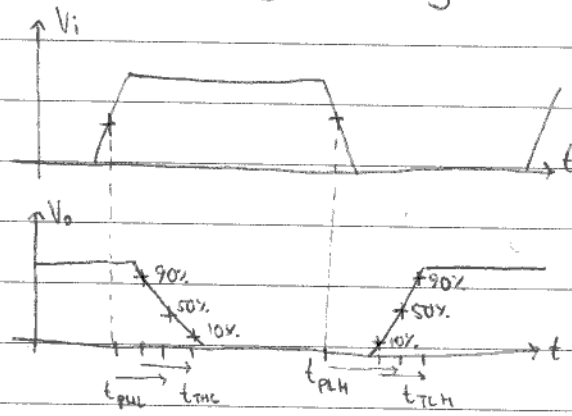
Case study - the CMOS 74HC00 (=D▷▷) NAND gate



Fan-out is determined by load capacitance & speed.

NOTES - Week 3: Rise time & Gate Delays

Rise-time & propagation delay: E.g. 74L500 —Do—



From DS, t_{PHL}, t_{PLH} } 15ns

But never use faster logic than you need!

$t_{TLH} = t_2 - t_1 = RC \ln 9 = 19ns$ (74HC00)

Definition (i) FAN-OUT is (of a logic gate) the output - the number of gate inputs to which it is connected. The maximum fan-out of a logic gate's output measures its load-driving capability: the greatest number of inputs of gates which the output can be safely connected.

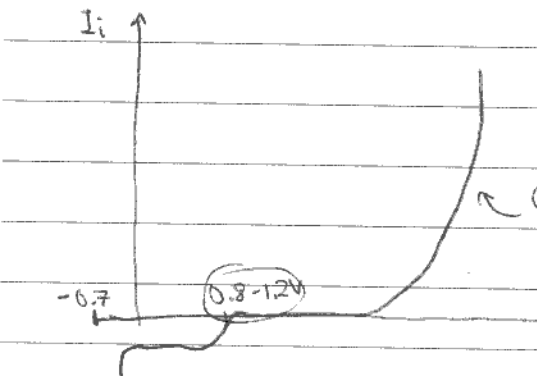
TTL:	I_{OH} sourcing	-0.4mA	I_{OL} sinking	16mA
	I_{IH} sinking	40μA	I_{IL} sourcing	-1.6mA

As far as formulae go, fan out = $\min\left[\left(\frac{I_{OL}}{I_{IL}}\right), \left(\frac{I_{OH}}{I_{IH}}\right)\right]$ (usually this)

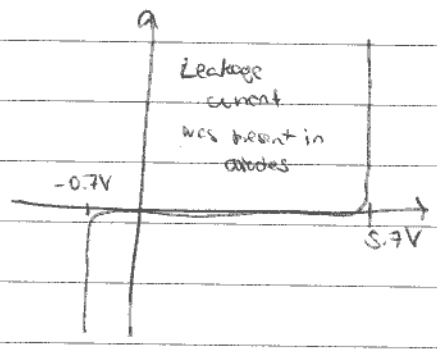
I/O current levels in CMOS logic: $I_i = \pm 1\mu A$ | $I_o = \pm 2.5mA$

For a $V_{DD} = 4.5V \longrightarrow V_{OL} = 0.33V$ at 4mA

TTL input characteristics (no Schottky!)



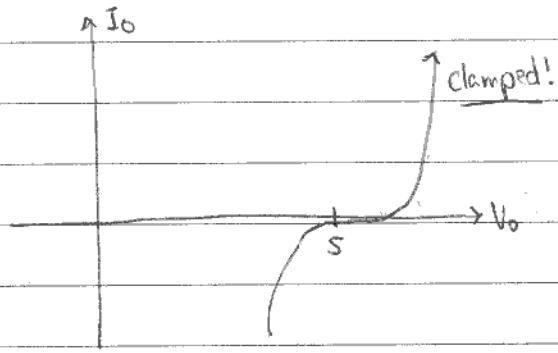
CMOS input characteristics (w protection diodes)



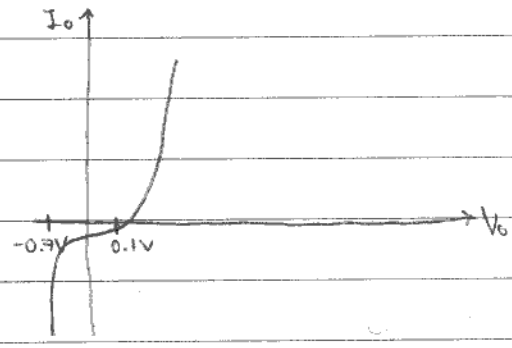
NOTES - Week 3: TTL and CMOS characteristics

TTL output characteristics:

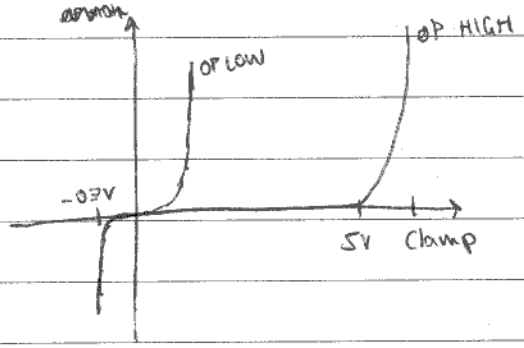
- Output high

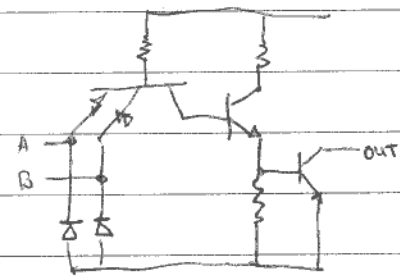


- Output low

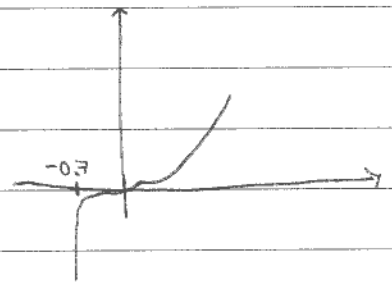


TTL open collector

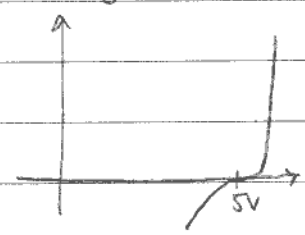




O/P Low



O/P High



Make sure fan out and noise margin are taken into consideration!